

LSLS/LSRS/ASRS r1, r2, #imm5

ADDS/SUBS r1, r2, r3

ADDS/SUBS r1, r2, #imm3

MOVS/CMP/ADDS/SUBS r1, #imm8

LDR r1, [pc, #4*imm8] (aka LDR r1, =const)

STRx/LDRx r1, [r2, r3]

STRx/LDRx r1, [r2, #s*imm5]

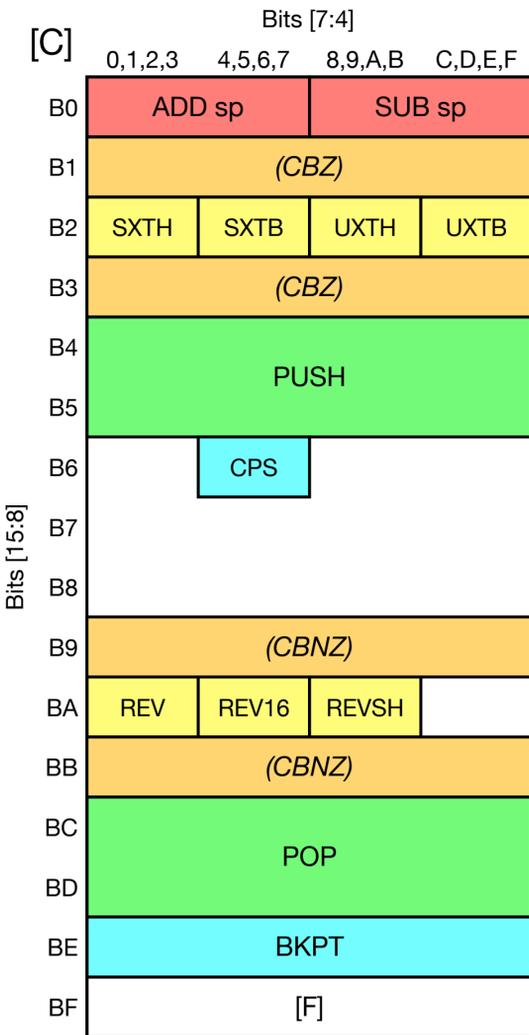
STR/LDR r1, [sp, #4*imm8]

ADD r1, pc, #4*imm8 (aka ADR r1, label)

ADD r1, sp, #4*imm8

STM/LDM r1!, {regs}

B 2*disp11



ADD/SUB sp, sp, #4*imm7

(CBZ r1, 2*disp5)

SXTH/SXTB/UXTH/UXTB r1, r2

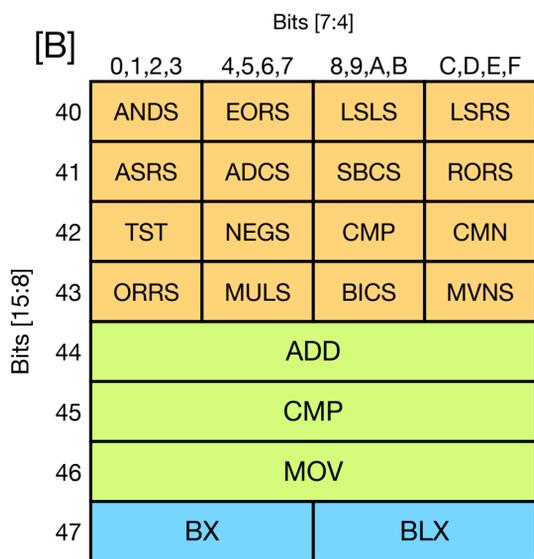
PUSH/POP {regs}

CPSIE/CPSID i

(CBNZ r1, 2*disp5)

REV/REV16/REVSH r1, r2

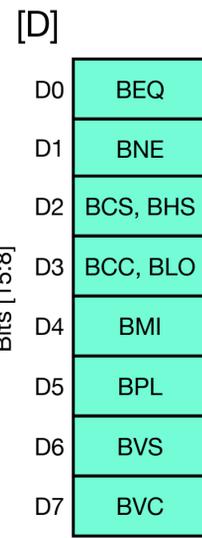
BKPT #imm8



op r1, r2

ADD/CMP/MOV r/h1, r/h2

BX/BLX r/h1



Bcc 2*disp8

SVC #imm8

[E] 32-bit instructions:

F38x 88xx MSR special, r1
 F3EF 8xxx MRS r1, special
 F3BF8F4x DSB
 F3BF8F5x DMB
 F3BF8F6x ISB
 Fxxx Fxxx BL 2*disp22

[F] Special instructions:

BF80 NOP
 BF90 YIELD
 BFA0 WFE
 BFB0 WFI
 BFC0 SEV
 BF?? (ITEcc)